Complete Sliced Model of Microwave FET's and Comparison with Lumped Model and Experimental Results

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Abstract— **This paper describes a rigorous and systematic procedure to derive a unified and complete semidistributed FET model that can be easily implemented in CAD routines of simulators. We have used the three coupled-line theory, including active and passive electromagnetic coupling between the semiconductor electrodes. The analytical formulas are given in order to calculate the capacitances of the electrodes and sufficient agreement is obtained in comparison with numerical analysis. For the first time, the experimental data of the device are compared with full three coupled-line theory and three coupled-line sliced model. This full semidistributed approach to FET modeling is applied to the analysis of a submicrometer-gate GaAs FET at centimeter and millimeter-wave frequencies, and the results are compared with the lumped element approach. The maximum available power gain (MAG) and the maximum stable power gain (MSG) of the device is calculated as a function of device width and frequency. Both the losses caused by the channel and those caused by the finite electrode conductivity are included. Good agreement is obtained between theory and experiment.**

I. Introduction

STATE-OF-THE-ART low-noise FET's (MESFET's and HEMT's) show transit frequencies of more than 100 GHz at submicron gate-length. FET modeling, on the other hand, does not keep pace with this rapid development due to problems in device measurement techniques and lack of basic theoretical work at the frequency range above 20 GHz.

For very-high frequency applications [21], [24], [27] the dimension of the transistor, in particular the electrode width, becomes comparable to the wavelength, λ_g. In such cases, wave propagation effects influence the electrical performance of the device.

Heinrich and Hartnagel [4], [26] reported on their study of the problem using the full-wave analysis technique and concluded that the distributed nature of electrodes becomes significant when the frequency is above 20 GHz. In this paper, a similar study is presented using coupled-mode theory [28] and a new semidistributed equivalent circuit based on distributed theory and experimental results, which can be integrated into a circuit simulator, is proposed. The electrodes are considered to be lossy transmission lines where their elements were calculated using numerical and analytical analysis. For the first time, each slice is represented by a 6-port equivalent circuit as shown in Fig. 3. The method of determining the values of the capacitance and inductance matrices is improved with sufficient accuracy. This modification is important because the wave propagation parameter (propagation constants, characteristic impedances, or admittances) depends on these elements. The lines are then modeled within the active parts of the transistor [13]. For purposes of simulation time reduction and thermal analysis of noise properties [22], [25], the complete sliced model with three coupled-lines consideration [1, 2] (instead of two coupled-lines analysis [10], [12], [18], [19], [20]) is proposed.

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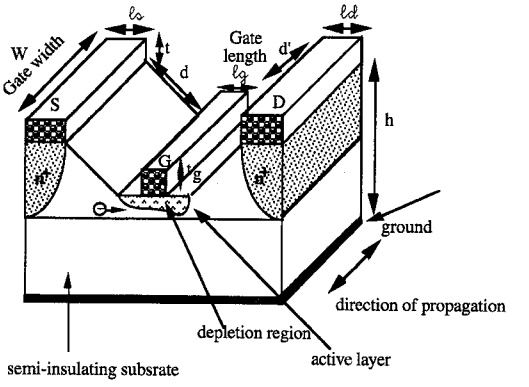


Fig. 1. Schematic showing the physical structure of MESFET with its important dimensions.

II. The Model and its Elements

A. Passive Electromagnetic Coupling

A schematic representation of a distributed MESFET is shown in Fig. 1. The device consists of three coupled electrodes fabricated on a thin layer of GaAs, supported by a semi-insulating GaAs substrate. The analysis of passive electromagnetic coupling are studied by two procedures, numerical and analytical analysis.

Numerical Analysis: In numerical analysis the device electrodes are considered as a multicoupled microstrip transmission line problem. For evaluating the self and inter-electrode capacitance of the system, Silvester's method was applied. In this method the whole problem of capacitance determination is divided into four steps [7], [14], [31]:

1) Finding the required Green's function.
2) Finding the Fredholm integral equation.
3) Applying the method of moments using Dirac delta functions as weighting functions (matrix approximation to integral equation).
4) Finding the matrix of Maxwell's potential coefficients and matrix of capacitances.

By repeating the calculation with the substrate dielectric equal to the free-space value, the inductance matrix may be obtained within the TEM approximation

$$[L] = \varepsilon_0 \mu_0 [C_0]^{-1}$$

with $[C_0]$ being the matrix of capacitances for the case where $\varepsilon_r = 1$. We compared our results with the literature [8], [9], [28], and good agreement was obtained.

Analytical Analysis: In our analytical approach the passive electromagnetic coupling elements are obtained from geometry and material constants of the FET and we assume that the gate-source and gate-drain spacing are equal. The Quasi TEM mode wave propagation of energy can be decomposed into an even and odd-mode excitation [12], [30], [31]. The even-mode wave transmission is analogous to excitation of a conductor-backed coplanar waveguide (CBCPW) and the odd-mode wave transmission is analogous to excitation of a pair of conductor-backed coplanar strips (CBCPS). With this description we can evaluate the capacitance matrix and then the inductance matrix of the system. The capacitance matrix is evaluated by using formulas in reference [5], [11] containing elliptic integrals.

For evaluating the capacitances C_{ss} and C_{dd} [see Fig. 3(c)] we have compared the numerical results with formulas that were used by Heinrich [3] but the values of the inductance did not show sufficient accuracy. For our problem the single narrow microstrip formulas [31], [30] are suitable and using these analytical formulas the capacitance and inductance matrices determination is improved.

B. Influence of Imperfect Conductors

For a conductor with finite thickness the surface impedance can be approximated as [6]

$$Z_s = z_m \coth(\gamma t) \tag{1}$$

where

$$\gamma = \frac{1+j}{\delta_m} \text{ is the propagation constant}$$

and

$$z_m = \frac{1+j}{\sigma_m \delta_m}$$

where $\delta_m = \sqrt{\frac{2}{\mu_0 \sigma_m \omega}}$ is the skin depth of metallic layers. This impedance can be separated into real and imaginary parts

$$Z_s = R_s + j\omega L s.$$

The real part represents the electrode resistance and the imaginary part the inner inductance. The surface resistance R_i and internal inductance L_i per unit length can be written as

$$R_i = \frac{\mathbf{R}e(z_m \coth(\gamma t))}{\mathbf{l}} \qquad L_i = \frac{\mathbf{I}m(z_m \coth(\gamma t))}{\mathbf{l}\omega}. \tag{2}$$

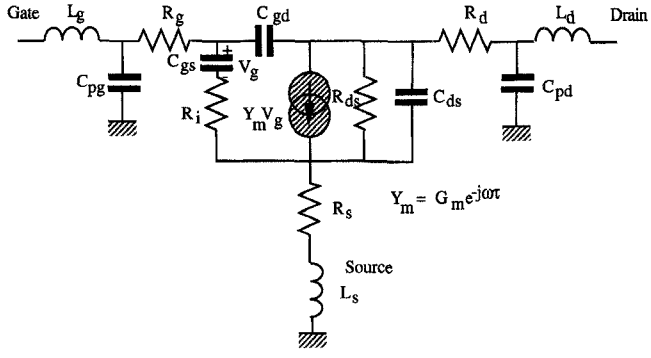


Fig. 2. Small-signal equivalent circuit of a FET.

In the case of FET electrodes we have

$$R_{ss} = \frac{\mathbf{R}e(z_m \coth(\gamma t))}{\mathbf{l_s}} \qquad l_s = \frac{\mathbf{I}m(z_m \coth(\gamma t))}{\omega \mathbf{l_s}}$$
$$R_{dd} = \frac{\mathbf{R}e(z_m \coth(\gamma t))}{\mathbf{l_d}} \qquad l_d = \frac{\mathbf{I}m(z_m \coth(\gamma t))}{\omega \mathbf{l_d}}$$
$$R_{gg} = \frac{\mathbf{R}e(z_m \coth(\gamma h_g))}{\mathbf{l_{gg}}} \qquad l_g = \frac{\mathbf{I}m(z_m \coth(\gamma h_g))}{\omega \mathbf{l_{gg}}}$$
$$\mathbf{l_{gg}} = \max\{\mathbf{l_g}, t_g\}, \qquad h_g = \min\{\mathbf{l_g}, t_g\} \tag{3}$$

with $\mathbf{l_s}$ = source length, $\mathbf{l_d}$ = drain length, $\mathbf{l_g}$ = gate length, t = source, and drain conductor thickness, t_g = gate conductor thickness.

C. Determination of Lumped Model of the FET

The broadband lumped model (Fig. 2) of the device was obtained using hot and cold modeling [15]–[17], [23]. In cold modeling the extrinsic elements $(L_g, C_{pg}, L_s, L_d, C_{pd})$ were extracted at ($V_{ds} = 0$ V, $V_{gs} = -4$ V) and ($V_{ds} = 0$ V, $V_{gs} > 0$ V) these elements being independent of frequency and of the biasing conditions. In hot modeling the intrinsic elements $(C_{gs}, C_{gd}, C_{ds}, G_m, R_i, R_{ds}, \tau)$ were obtained by the de-embedding procedure of extrinsic elements. The intrinsic elements are independent of the frequency but they are functions of bias conditions. Optimization was performed by varying the values of the intrinsic FET elements in the vicinity of $\pm 10\%$ of their mean value until the error between measured and modeled S-parameters were reduced to acceptable levels.

D. Determination of the Distributed Model of the FET

In the distributed model (full sliced model), the FET is divided into many cells cascaded together, as shown in Fig. 3(a)–(c). Each cell contains the coupled electrode transmission lines, resistance and internal inductance of electrodes, and an intrinsic GaAs FET equivalent circuit. The values of coupled transmission line elements, resistance and internal inductance of electrodes have been given in (3). To deduce the values of C_{pgd} and C_{pdd} at the input and output of the distributed FET model, the capacitances C_{11} and C_{22} are subtracted from the corresponding capacitances C_{pg} and C_{pd} of the lumped FET model as follows

$$C_{pgd} = (C_{pg} - C_{11})N/2 \qquad C_{pdd} = (C_{pd} - C_{22})N/2 \tag{4}$$

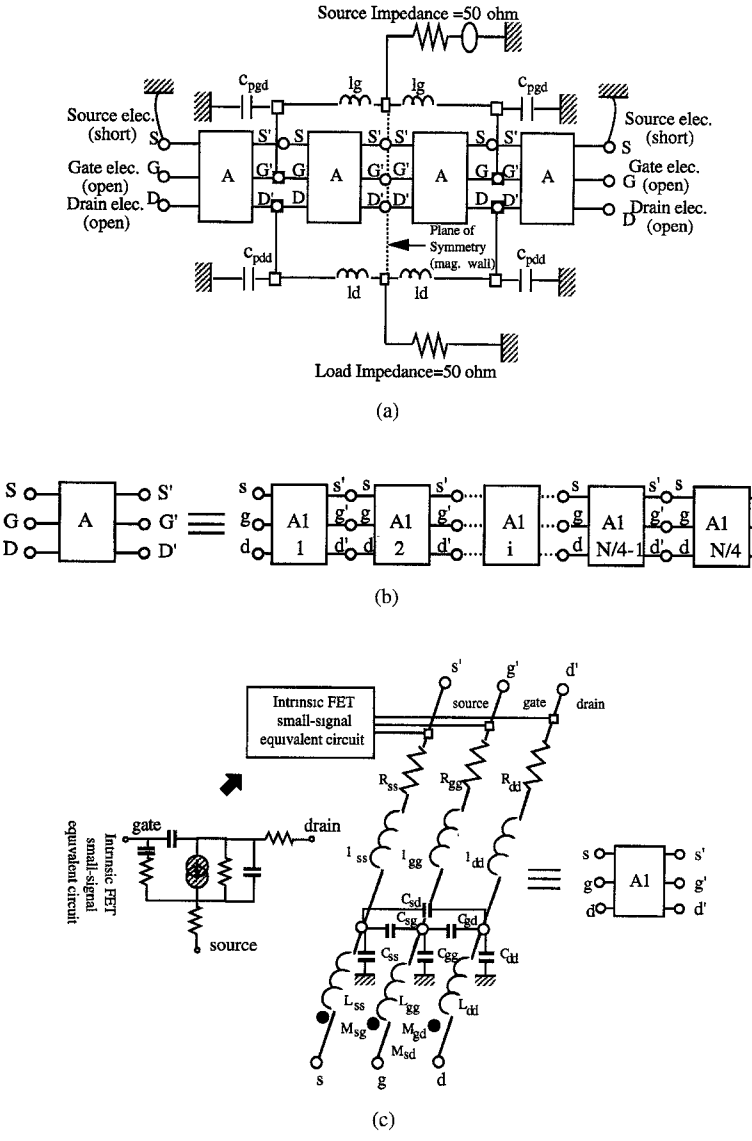


Fig. 3. Complete detailed circuit diagram for our FET distributed model: (a) Full sliced model representation of a pi-gate FET, (b) representation of a quarter of the FET by cascaded six-port cells, and (c) an elementary cell of distributed FET configuration.

where

$$C_{11} = C_{gg} + \frac{C_{sg}C_{ss}}{C_{ss} + C_{sd} + C_{sg}}$$
$$C_{22} = C_{dd} + \frac{C_{sd}C_{ss}}{C_{ss} + C_{sd} + C_{sg}} \quad (5)$$

N is slice number. The value of l_g and l_d in the distributed FET model in Fig. 3(a) are chosen as

$$l_g \approx 2L_g, \quad l_d \approx 2L_d$$

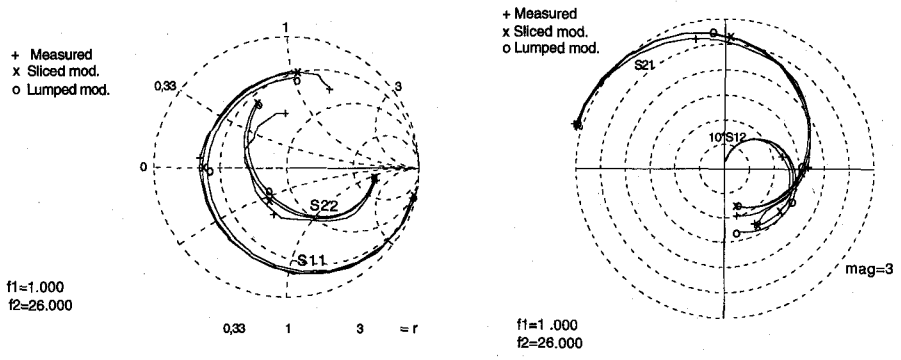
where L_g and L_d are the extrinsic inductances in the lumped FET model (Fig. 2). Scaling rules were applied to the other elements of the lumped model, as shown in Table I, in order to obtain the element values of the intrinsic FET small-signal equivalent circuit cell in Fig. 3(c). The value of C_{21} in Table I is given by

$$C_{21} = C_{dg} + \frac{C_{sg}C_{sd}}{C_{ss} + C_{sd} + C_{sg}}.$$

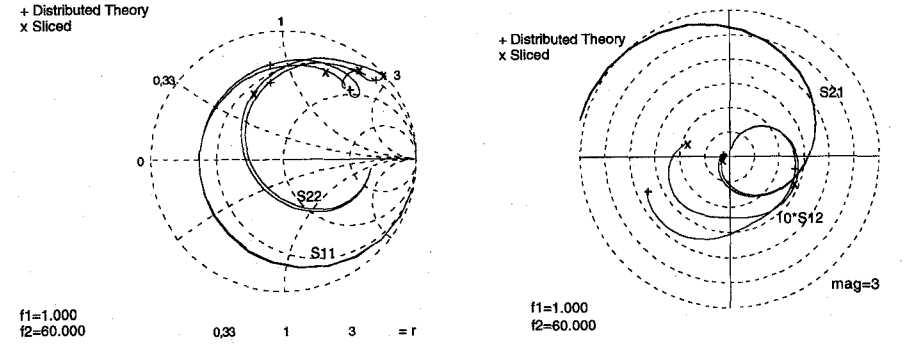
TABLE I
LINEAR SCALING RULES FROM LUMPED MODEL TO DISTRIBUTED MODEL

Lumped model	Distributed model
Cgs	Cgs/N
Cgd	(Cgd-C21)/N
Cds	Cds/N
Rds	Rds*N
Ri	Ri*N
Gm	Gm/N
Tau	Tau
Rg	3*Rg/N
Rd	Rd*N-Rdd
Rs	Rs*N-Rss

From several computations of the distributed FET models for $W = 4\times70 = 280$ micrometers, a value of $N = \frac{\text{Gate Width}}{\text{Slice Width}} = 4$ has been chosen and used in all the simulations. For $N > 4$, results of S-parameter simulations remain approximately identical.



(a)



(b)

Fig. 4 (a) Comparison between measured and modeled S-parameters in the range 1–26 GHz. Device NE710 $I_{ds} = 10$ mA; $V_{ds} = 3$ V. (b) Comparison between distributed theory and sliced model S-parameters in the range 1–60 GHz.

TABLE II
NUMERICAL VALUES OF LUMPED MODEL ELEMENTS $V_{ds} = 3$ V, $I_{ds} = 10$ mA

Lumped model elem.	Numerical Value	
Cgs	0.216	pF
Cgd	0.033	pF
Cds	0.005	pF
Rds	231	ohm
Ri	7.3	ohm
Gm	41	mS
tau	1.98	pS
Rg	3.29	ohm
Rd	1.77	ohm
Rs	1.74	ohm
Lg	0.383	nH
Ld	0.434	nH
Ls	0.094	nH
Cpg	0.078	pF
Cpd	0.092	pF

TABLE III
NUMERICAL VALUES OF DISTRIBUTED MODEL ELEMENTS $V_{ds} = 3$ V, $I_{ds} = 10$ mA

Distributed model elem.	Numerical Value	
Int. FET small-signal equivalent circuit	See tables I and II	
Rss =Rdd	0.9	ohm/mm
Rgg	34.3	ohm/mm
lss=ldd	0.06	nH/mm
lgg	0.12	nH/mm
Lss=Ldd	0.72	nH/mm
Lgg	1.49	nH/mm
Msg=Mgd	0.36	nH/mm
Msd	0.24	nH/mm
Css=Cdd	0.087	pF/mm
Cgg	0.0006	pF/mm
Csg=Cgd	0.029	pF/mm
Csd	0.061	pF/mm

III. RESULTS

This procedure was used for complete small-signal characterisation of a submicrometer-gate GaAs NE710 transistor. The NE710 is a transistor for low-noise applications. The device has a 0.3 μm $\times$ 280 μm gate with a "pi-gate" shape. Both the input and output nodes were connected to the centre of the gate and drain electrodes. The transistor was biased at $V_{ds} = 3$ V, $I_{ds} = 10$ mA and the S-parameters were measured in 1–26 GHz band using the HP 8510 C Network analyzer. The values of lumped model elements and distributed model elements are shown in Tables II and III. In Fig. 4(a) the S-parameters of the sliced model, measured data, and lumped model data have been compared in 1–26 GHz band at $V_{ds} = 3$ V, $I_{ds} = 10$ mA bias point. Comparing these curves, one can see that the sliced model is better when compared with measured data in this frequency band. To validate the sliced model with the distributed theory model, Fig. 4(b) is presented and one can see that these results are comparable in this frequency band, except for S_{12}.

Using the device fabrication data sheet and its geometry consideration (Fig. 1), the values for the various device

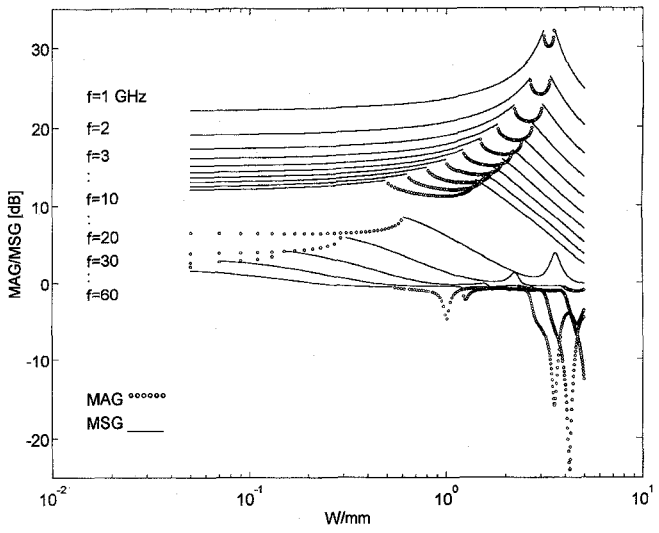


Fig. 5. Maximum available gain (MAG) and maximum stable gain (MSG) as a function of the gate width W at different frequency.

dimensions and material constants were chosen as follows:

$$\mathrm{l_s}(\text{source length}) = \mathrm{l_d}(\text{drain length}) = 24\ \mu\text{m},$$
$$\mathrm{l_g}(\text{gate length}) = 0.3\ \mu\text{m},\ h(\text{electrode's height}) = 140\ \mu\text{m},$$
$$d(\text{source-gate separation}) = d'(\text{gate-drain separation}) = 2\ \mu\text{m},$$
$$W(\text{gate width}) = 280\ \mu\text{m},\ t = t_g = 2\ \mu\text{m},$$
$$\varepsilon_r = 12.9,\ \sigma_m = 4.10^7(\Omega\cdot\text{m})^{-1}.$$

For evaluating the performance potential of the device, the maximum available gain (MAG) and the maximum stable gain (MSG) are presented in Fig. 5. At some values of gate width and frequency, no MAG can be defined, because the transistor under consideration is merely conditionally stable (the Rollet constant K is smaller than 1). In these cases, the MSG has been computed instead. At low frequencies by increasing the gate width, MAG can be defined and then simultaneously conjugate matching the input and output ports of the final two-ports [29]. Fig. 5 gives this idea that MAG can be defined for each frequency when the gate width is in the corresponding range. The information obtained from these two figures of merit (MAG and MSG) should be useful for making foundry decision and evaluating the performance potential of newly developed devices.

IV. Conclusion

A full distributed theory and full sliced FET model (with three coupled-line consideration) are presented and compared. The advantages of full sliced model is indicated and used in all the simulations. Using this modeling method, the characteristic impedance or admittance of the electrodes for each mode are obtained which are useful for achieving high maximum available gain with suitable termination at the end of each electrode [28]. This method can be applied to full sliced linear and nonlinear (using the nonlinear intrinsic FET element model) [10] modeling of any MESFET or HEMT at millimeter-wave frequency. Such procedure is also useful for noise analysis of FET's which allows the prediction of noise parameters at millimeter-wave frequency and therefore simultaneously determination of signal and noise parameters for CAD applications. The noise analysis results will be published in a future communication. Finally, using this method the optimization of the device geometry for improving its performance is possible.

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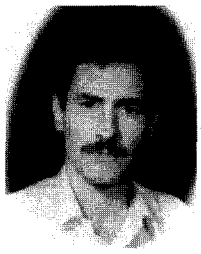
References

[1] V. K. Tripathi, "Asymmetric coupled transmission lines in an inhomogeneous medium," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-23, pp. 734–739, 1975.
[2] ——, "On the analysis of symmetrical three-line microstrip circuits," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-25, pp. 726–728, 1977.
[3] W. Heinrich, "Distributed equivalent-circuit model for travelling-wave FET design," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-35, pp. 487–491, 1987.
[4] W. Heinrich and H. L. Hartnagel, "Field theoretical analysis of wave propagation on FET electrodes including losses and small signal amplification," *Int. J. Electronics*, vol. 58, pp. 613–627, 1985.
[5] G. Ghione and C. Naldi, "Parameters of coplanar waveguides with lower ground plane," *Electron. Lett.*, vol. 19, pp. 734–735, Sept. 1983.
[6] D. Jager, "Slow-wave propagation along variable Schottky-contact microstrip line," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-24, pp. 566–573, 1976.
[7] P. Silvester, "TEM wave properties of microstrip transmission lines," in *Proc. IEE*, 1968, vol. 115, pp. 43–48.
[8] N. G. Alexopoulos, J. A. Maupin, and P. T. Greiling, "Determination of the electrode capacitance matrix for GaAs FET's," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-28, pp. 459–466, 1980.
[9] A. K. Goel, "Electrode parasitic capacitances in self-aligned and deep-recessed GaAs MESFET's," *Solid-State Electron.*, vol. 31, pp. 1471–1476, Sept. 1988.
[10] E. Ongareau, R. G. Bosisio, M. Aubourg, J. Obregon, and M. Gayral, "A nonlinear and distributed modeling procedure of FET's," *Int. J. Numerical Modeling*, vol. 6, pp. 237–251, 1993.
[11] S. M. Wentworth, D. P. Neikirk, and C. R. Brahce, "The high-frequency characteristics of tape automated bonding (TAB) interconnects," *IEEE Trans. Components, Hybrids, Manufact. Technol.*, vol. 12, pp. 340–346, 1989.
[12] R. L. Chang, T. J. Shieh, W. A. Davis, and R. L. Carter, "Modeling and analysis of GaAs MESFET's considering the wave propagation effect," in *IEEE MTT-S Dig.*, vol. MTT-28, 1989, pp. 371–374.
[13] A. J. Holden, D. R. Daniel, I. Davies, C. H. Oxley, and H. D. Rees, "Gallium arsenide travelling-wave field-effect transistors," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 61–66, 1985.
[14] R. F. Harrington, *Field Computation by Moment Methods*. New York: Macmillan, 1968.
[15] G. Dambrine, A. Cappy, F. Heliodore, and D. Playez, "A new method for determining the FET small-signal equivalent circuit," *IEEE Trans. Microwave Theory Tech.*, vol. 36, pp. 1151–1159, 1988.
[16] N. Berroth and R. Bosch, "Broad-band determination of the FET small-signal equivalent circuit," *IEEE Trans. Microwave Theory Tech.*, vol. 38, pp. 891–895, 1990.
[17] R. Tayrani, J. Gerber, T. Daniel, R. S. Pengelly, and U. L. Rohde, "Reliably extract MESFET and HEMT parameters," *Microwaves & RF*, pp. 131–135, June 1993.
[18] L. Escotte and J. C. Mollier, "Semidistributed model of millimeter-wave FET for S-parameter and noise figure predictions," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-38, pp. 748–753, 1990.
[19] A. S. Podgorski and L. Y. Wei, "Theory of travelling-wave transistors," *IEEE Trans. Electron Devices*, vol. ED-29, pp. 1845–1853, 1982.

[20] R. Larue, C. Yuen, and G. Zdasiuk, "Distributed GaAs FET circuit model for broadband and millimeter wave applications," in *IEEE MTT-S Dig.*, 1984, pp. 164–166.
[21] R. L. Kuvas, "Equivalent circuit model of FET including distributed gate effects," *IEEE Trans. Electron Devices*, vol. 27, pp. 1193–1195, 1980.
[22] M. W. Pospieszalski, "Modeling of noise parameters of MESFET's and MODFET's and their frequency and temperature dependence," *IEEE Trans. Microwave Theory Tech.*, vol. 37, pp. 1340–1350, 1989.
[23] R. Anholt and S. Swirhun, "Measurement and analysis of GaAs MESFET parasitic capacitances," *IEEE Trans. Microwave Theory Tech.*, vol. 39, pp. 1247–1251, 1991.
[24] W. Heinrich, "Limits of FET modeling by lumped elements," *Electron. Lett.*, vol. 22, pp. 630–632, 1986.
[25] M. T. Hickson, P. Gardner, and D. K. Paul, "A semidistributed Touchstone model for the noise and scattering parameters of a HEMT," *UMIST*, 1993.
[26] W. Heinrich and H. L. Hartnagel, "Wave propagation on MESFET electrodes and its influence on transistor gain," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-35, pp. 1–8, 1987.
[27] P. H. Ladbrooke, "Some effects of wave propagation in the gate of a microwave MESFET," *Electron. Lett.*, vol. 14, pp 21–22, 1978.
[28] A. Abdipour, "Report intern," *Supélec*, 1993.
[29] A. Pacaud, "Electroniqe," *École Supérieure d'Électricité*, 1992.
[30] T. Edwards, *Foundations for Microstrip Circuit Design*, 2nd ed. New York: Wiley, 1992.
[31] K. C. Gupta, R. Garg, and I. J. Bahl, *Microstrip Lines and Slotlines*. Norwood, MA: Artech House, 1979.



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